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(71) Applicant (for all designated States except US): **KONINKLIJKE PHILIPS ELECTRONICS, N.V.** [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(71) Applicant (for AE only): **U.S. PHILIPS CORPORATION** [US/US]; 1251 Avenue of the Americas, New York, New York 10020 (US).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **DONKERS, Johannes J.T.M.** [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL). **MAGNEE, Petrus, H., C.** [NL/BE]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL). **KUNNEN, Eddy** [BE/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL). **NEUILLY, Francois, I.** [FR/BE]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

(74) Common Representative: **KONINKLIJKE PHILIPS ELECTRONICS, N.V.**; c/o Waxler, Aaron P.O. Box 3001, Briarcliff Manor, NY 10510-8001 (US).

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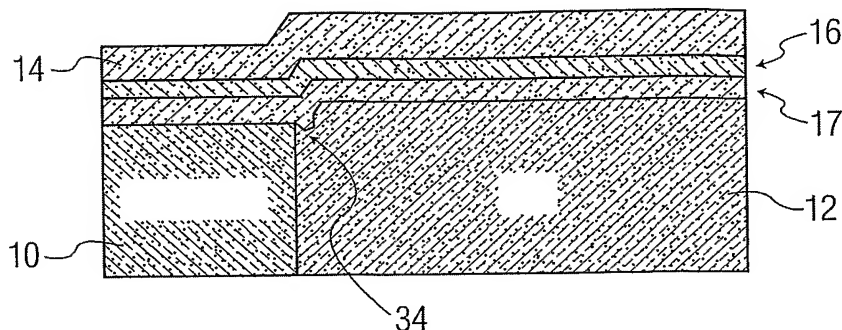
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— as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA,

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(54) Title: METHOD TO REDUCE SEEDLAYER TOPOGRAPHY IN BICMOS PROCESS



(57) Abstract: A method for forming an epitaxial base layer in a bipolar device. The method comprises the steps of: providing a structure having a field isolation oxide region (12) adjacent to an active silicon region (10); forming a silicon nitride/silicon stack (14, 16) above the field isolation oxide region (12), wherein the silicon nitride/silicon stack (14, 16) includes a top layer of silicon (14) and a bottom layer of silicon nitride (16); performing an etch to the silicon nitride/silicon stack (14, 16) to form a stepped seed layer, wherein the top layer of silicon is etched laterally at the same time the bottom layer of silicon nitride is etched; and growing an Si/SiGe/Si stack (20) over the stepped seed layer and active region (10).

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